Amendments to the Claims

1. (Previously Presented) A device comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a gate, source, and drain;

wherein the bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

2. - 8. (Cancelled)

9. (Currently Amended) A device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a third field effect transistor having a gate, source, and drain, wherein the sources and drains of the first and second field effect transistors and the drain and gate of the third field effect transistor are all connected to each other, and wherein the gates of the first and second field effect transistors are not connected to each other.

10. (Currently Amended) The device as set forth in claim 9, wherein an impedance looking into ~~between~~ the gates of the first and second field effect transistors is substantially capacitive.

11. (Currently Amended) A device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a bipolar transistor having a base, emitter, and collector, wherein the sources and drains of the first and second field effect transistors and the base and collector of the bipolar transistor are all connected to each other, wherein the gates of the first and second field effect transistors are not connected to each other.

12. (Currently Amended) The device as set forth in claim 11, wherein an impedance looking into ~~between~~ the gates of the first and second field effect transistors is substantially capacitive.

13. (Currently Amended) An amplifier comprising:

an output stage having an output port and an input port; and

a device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a third field effect transistor having a gate, source, and drain, wherein the sources and drains of the first and second field effect transistors and the drain and gate of

the third field effect transistor are all connected to each other, wherein the gates of the first and second field effect transistors are not connected to each other;

wherein the gate of the first field effect transistor is connected to the output port and the gate of the second field effect transistor is connected to the input port.

14. (Original) The device as set forth in claim 13, wherein the output stage comprises a field effect transistor having a gate and a drain, wherein the gate of the output stage is connected to the input port and the drain of the output stage is connected to the output port.

15. (Currently Amended) An amplifier comprising:

an output stage having an output port and an input port; and

a device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a bipolar transistor having a base, emitter, and collector, wherein the sources and drains of the first and second field effect transistors and the base and collector of the bipolar transistor are all connected to each other, and wherein the gates of the first and second field effect transistors are not connected to each other;

wherein the gate of the first field effect transistor is connected to the output port and the gate of the second field effect transistor is connected to the input port.

16. (Original) The device as set forth in claim 15, wherein the output stage comprises a field effect transistor having a gate and a drain, wherein the gate of the output stage is connected to the input port and the drain of the output stage is connected to the output port.

17. (Previously Presented) A communication circuit comprising:

an amplifier comprising a capacitor to provide compensation, the capacitor comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a gate, source, and drain;

wherein the bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

18. - 20. (Cancelled)

21. (Previously Presented) A device comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a base, emitter, and collector;

wherein the bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect

transistors and the base and collector of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

22. (Previously Presented) A communication circuit comprising:

an amplifier comprising a capacitor to provide compensation, the capacitor comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a base, emitter, and collector;

wherein the bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the base and collector of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.